FIRMWARE RC21 · B0 SILICON ONLY

Switch Firmware

RC21 Release Notes

A Gen6 link-training and configuration-cleanup release.

Applies to Atlas3 PCIe Gen6 host cards built on B0 silicon, standard (high lane count) configurations, running in unmanaged mode.

Document Rev 1.0 · 16 November 2026

RELEASE SUMMARY

RC21 at a glance

RC21 brings in the switch vendor's RC19–RC21 updates: a workaround for Gen6 links that skip equalization, new link-management microcode and a 75 W straddle slot.

ITEM	THIS RELEASE
Firmware revision	RC21
Supersedes	RC18 (previous general release)
Release date	14 November 2026
Silicon	B0 only
Image type	Unmanaged-mode switch configuration image (miniSBR + signed mainSBR)
Image file	PCI6-AD-X16HI-BG6-80_B0_RC21_UnMgd_4_mode_rsa.imd.signed
Version word suffix	**B015** (RC18 ended in B012)

> WHAT "SWITCH FIRMWARE" MEANS HERE
>
> In unmanaged mode the switch firmware is the boot-time configuration image that the switch loads from its on-card storage: link and PHY tuning, port layout, clocking mode, and the embedded link-management microcode. There is no separate run-time firmware to update.

APPLICABILITY

Which cards this release covers

This release is silicon-specific. Confirm the silicon revision of every card before you transfer an image to it.

	SCOPE
Applies to	Atlas3 PCIe Gen6 host cards built on B0 silicon, in standard (high lane count) configurations — 80-lane operating in unmanaged mode.
Does not apply to	Cards built on A0 silicon, and low lane count (LLC) Atlas3 host cards. Those use a separate image set with its own revision numbering.

WHO SHOULD UPDATE

Upgrade if any of these apply

- You see Gen6 links reach 64 GT/s without passing through equalization.
- An add-in card in the x16 straddle connector (CN1) that needs more than 25 W, or whose driver limits performance because of the reported slot power.
- You are starting a new qualification of Gen6 endpoints, cables or retimers.

> **RECOMMENDATION**
> If your Gen6 links are stable on RC18 and your software does not depend on PCI addresses or slot attributes, you can schedule this update with your next qualification cycle. **RC21 is the recommended baseline for all new validation work.**

CHANGE DETAIL

What changed

RC21 is cumulative over RC18 and rolls up the switch vendor's RC19, RC20 and RC21 updates. RC19 adds nothing new for B0 host cards; its settings already shipped in RC18.

RC20 and RC21 — link behavior

AREA	CHANGE	BENEFIT
Gen6 training without equalization	RC21 adds a workaround for links that could train to 64 GT/s without passing through equalization. Four link-training and PHY safety settings are applied at boot, including the equalization far-end wait count and transmitter-adaptation timing.	Addresses links that reach 64 GT/s without completing equalization.
Gen6 adaptation preset	Gen6 transmitter adaptation now starts from preset 2 instead of preset 5, on all ports.	Matches the vendor's production Gen6 equalization setting.
Lane margining	RC20 adjusts the Gen6 lane-margining limits (maximum timing offset).	Gen6 margining runs within the vendor's recommended limits.
SerDes tuning	RC20 updates the SerDes analog front-end thresholds and the PIPE transmit-control and timing-evaluation settings. All four modes receive the same changes.	Latest vendor hardware recommendations for the SerDes.
Link-management microcode	Both embedded microcode images were updated, the first change since RC15. They match the vendor's current production release bit for bit.	Current vendor link-training and link-management code.

RC21 — changes software can see

AREA	CHANGE	EFFECT
Straddle slot (CN1, port 16)	Now reports a 75 W slot power limit with no hot-plug capability or attention indicator. RC18 reported 25 W, hot-plug capable.	An add-in card that needs more than 25 W is no longer told the slot cannot power it. Connect CN8 auxiliary power for 75 W operation.
MCIO slot attributes (ports 0–14, 32–46)	No attention indicator is advertised, and the No Command Completed Support bit is now clear. Slot power limit (25 W) and hot-plug capability are unchanged.	Slot attributes match the card, which has no attention indicators.
Downstream device numbers	Straddle port back at device 08h on the switch's internal bus and internal MCIO ports (CN3, CN5) at 09h–10h, as in RC15. RC18 had them at 10h and 08h–0Fh. External MCIO ports (CN2, CN4) unchanged.	PCI addresses of the straddle and internal MCIO ports, and devices behind them, differ from RC18 (see the caution below).

RC21 — configuration cleanup

AREA	CHANGE	EFFECT
Reference-kit slot settings	Reference-kit slot power limits on ports 64, 80, 96 and 128, and the slot-implemented overrides on ports 80, 96, 112 and 128, were removed.	Settings that applied only to the reference kit are gone.
Reference-kit GPIO settings	The reference-kit GPIO-to-port map in the boot header was cleared, keeping only the entries this card uses, and the reference-kit SBR-load GPIO sequence was removed.	The image carries only settings for the 80-lane host card.
Lane equalization block	A duplicate block of lane-equalization preset writes was removed. The remaining block holds the same final values.	No net change; a shorter configuration.
Other settings	The SPI flash-mode field returns to its RC15 setting, and one board-specific write was added on the golden-finger upstream port (port 96).	Board-level settings for this card.
Image identity	The file name drops “RDK104”. The version word ends in B015.	Signed with the same RSA-4096 key as RC18, so no new key migration is needed.

COMPATIBILITY

What did not change

RC21 keeps the configuration framework of RC18. The following are unchanged:

- Port layout, upstream and downstream assignment, and lane widths in every mode. Only the downstream device numbering changed (see the caution below).
- The four selectable modes (common clock or SRNS on the golden finger, precoding on or off) and the clocking of every port. Clocking mode is still applied only at switch boot.
- PCI identification: vendor, device and subsystem IDs.
- The secure boot signing key: RSA-4096, the same key as RC18.
- The miniSBR. **Only the mainSBR needs to be updated when moving from RC18 or RC15 to RC21.**
- The on-card storage layout.

> **CAUTION — DOWNSTREAM DEVICE NUMBERS CHANGED FROM RC18**
> RC21 restores the RC15 device numbering: the straddle port is device 08h and the internal MCIO ports are devices 09h–10h on the switch’s internal bus. If your scripts or host configuration identify the straddle or internal MCIO ports, or the devices behind them, by PCI bus, device or function number, update them. **External MCIO ports (CN2, CN4) keep the same addresses.**

UPDATE PROCEDURE

Upgrade notes

The steps below describe an RC18 to RC21 update; coming from RC15 is the same. Rolling back to RC18 uses the same procedure, so keep a copy of the RC18 image.

1. **Match the image to card silicon.** Use a B0 image on B0 cards only.
2. **Update the MCU firmware image to v0.1.4**
   - **a.** From the MCU CLI, run the **‘fdl mcu’** command
   - **b.** Upload the v0.1.4 image via XMODEM (Located in the MCU folder)
     - TeraTerm: File > Transfer > XMODEM > Send
     - minicom: Ctrl + A > Press ‘s’ > Upload Menu > xmodem > Enter
     - Run the **‘reset’** command

3. **Update the mainSBR.** The miniSBR does not need to be re-flashed when coming from RC18 or RC15.
   a. From the MCU CLI, run the **'fdl main'** command, confirm the erase
   b. Upload the RC21 image via XMODEM (Located in the FW folder)
      - TeraTerm: File > Transfer > XMODEM > Send
      - minicom: Ctrl + A > Press 's' > Upload Menu > xmodem > Enter
4. **Power-cycle the card after the transfer.** The switch reads this image only at power-on; a warm reset or a link retrain does not apply it.
5. **Confirm the version.** After power-up, check that the reported version word ends in B015.
6. **Re-run link qualification.** Speed and width, equalization results and BER should all be re-measured. PHY tuning and link-management microcode changed in this release, so margins recorded on RC18 are not directly comparable.

PREREQUISITE — SECURE BOOT KEY MIGRATION

RC21 images are signed with the same RSA-4096 key as RC18. A card already running RC18 has completed the one-time secure boot key migration and needs nothing further. A card that has not been migrated will not authenticate this image: perform the migration first, then return to the steps above.

See: **Atlas3 B0 Secure Boot Key Migration** (separate procedure document).

UPGRADING FROM RC9 OR EARLIER

These notes describe an RC18 to RC21 update. Moving up from the RC9 generation also picks up everything introduced in RC15, including the first release of the embedded link-management microcode and a revised miniSBR. Complete the key migration, then flash **both the miniSBR and the mainSBR**.

TALK TO US

Questions about this release?

Serial Cables applications engineering can help you plan the update, interpret link qualification results on the new PHY tuning, or supply the previous image for rollback.

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ADDENDUM A

Firmware revision history

This addendum records every B0 switch firmware revision released to date, newest first. It is maintained in place: as each new revision is published, a row is added to the summary below and a change table is added above the current top entry, so this document always carries the full history.

Revision summary — B0 silicon, standard (high lane count) configurations

REVISION	RELEASED	VERSION WORD	STATUS
RC21	November 2026	**B015**	**Current general release**
RC18	August 2026	**B012**	Previous general release
RC15	July 2026	**B00F**	Interim pre-release
RC9	April 2026	**B009**	Earlier general release

RC21 — November 2026 · current general release (see "What changed")

AREA	CHANGE	BENEFIT
Gen6 equalization	Workaround for links that could train to 64 GT/s without passing through equalization; Gen6 adaptation starting preset changed from 5 to 2.	Addresses links that reach 64 GT/s without completing equalization.
Gen6 PHY tuning	Gen6 lane-margining limits, SerDes front-end thresholds and PIPE transmit settings updated, identically in all four modes.	Latest vendor hardware recommendations.
Link-management microcode	Both microcode images updated, the first change since RC15.	Current vendor link-training code.
Slot attributes	Straddle slot (port 16) now 75 W, not hot-plug capable. MCIO slots no longer advertise an attention indicator; No Command Completed Support cleared.	Slot attributes match the hardware.
Device numbering	Straddle back at device 08h, internal MCIO ports at 09h–10h, as in RC15.	Reverts the RC18 change.
Reference-kit cleanup	Reference-kit slot, GPIO and SBR-load settings removed; duplicate lane-equalization block removed. File name drops "RDK104".	Image specific to the 80-lane host card.
Image signing	Same RSA-4096 key as RC18.	No new key migration.

RC18 — August 2026 · rolls up RC16 and RC17

AREA	CHANGE	BENEFIT
Gen6 speed change	Rate-change pacing corrected, and precoding state cleared whenever the link passes through Detect.	Fixes Gen6 rate-change failures with specific link partners, and post-retrain instability at 64 GT/s.
Gen6 clock recovery	CDR phase-step reduced from 4 to 2; a 10 µs CDR re-lock delay added after electrical idle exit; RX loss-of-signal filter retuned.	Tighter Gen6 clock-recovery tracking and fewer false signal-loss events on marginal channels.
Adaptive equalization	Adaptive-EQ starting gain reduced from 0x9 to 0x6; TX slew-rate control returned to its default (disabled).	Resolves a rate-change interoperability problem with certain host platforms.
PHY safety settings	Two additional sets of PHY and link-training safety settings are applied at boot.	Broader protection against link-training corner cases.
CDR gain workaround	The link-state-dependent CDR-gain workaround, enabled in RC15, is off by default again.	The receiver behaves the same in and out of L0, matching RC9 behavior.

RC18 — August 2026 · rolls up RC16 and RC17

AREA	CHANGE	BENEFIT
Configuration	Gen6 lane transmitter preset for upstream- and downstream-facing ports changed from 5 to 2. Straddle port moved from device 08h to 10h, and internal MCIO ports from 09h–10h to 08h–0Fh (restored in RC21). No change to port layout, lane widths or clocking mode.	Existing profiles keep their port layout.

RC15 — July 2026 · interim pre-release

AREA	CHANGE	BENEFIT
Link-management microcode	Microcode image updated, and a second, larger microcode image added. RC9 shipped that slot empty.	Carries the Gen6 link-training fixes developed since the beta and enables link-management functions the beta image did not have.
Gen6 PHY tuning	Most of the Gen6 PHY retune landed here — clock recovery, adaptive equalization and receiver signal detection.	Baseline Gen6 link robustness ahead of RC18.
Core voltage	The core-voltage scaling override that RC9 applied at boot was removed; the switch now uses its factory-programmed setting. This setting lives in the miniSBR.	Returns the part to its characterized operating point. Switch power and temperature readings may shift slightly.
PCI identification	The 104-lane and 80-lane profiles now report subsystem ID 0144 (subsystem vendor 1000); lane count moved to a dedicated setting.	One subsystem ID across all B0 configurations — see the caution below.
Image signing	The RSA-4096 signing-key update is delivered as an update to this package. The signed mainSBR is about 0.8 KB larger per profile.	Required before RC18 can be installed.
CDR gain workaround	The link-state-dependent CDR-gain workaround was enabled in this revision only.	Switched back off in RC18.
Packaging	Configuration schema moved from version 10 to version 11; a flash-mode selection field was added (default value, no behavior change); reference-kit profiles gained explicit 75 W slot power limits on four downstream slots.	Reference-kit power limits apply to the reference kit only.

RC9 — April 2026 · earlier general release

AREA	BEHAVIOR ON RC9
Baseline	First general release for B0 silicon.
Link-management microcode	Single beta microcode image; the second image slot was empty.
Core voltage	A core-voltage scaling override was applied at boot.
PCI identification	The 104-lane profile reported subsystem ID 0104; the 80-lane profile reported 0080.
Image signing	Images were signed with an elliptic-curve (ECDSA) key.

CAUTION — PCI SUBSYSTEM ID CHANGED AFTER RC9

If you are coming from RC9 and your software or scripts identify 104-lane or 80-lane configurations by PCI subsystem ID, update them. **All B0 standard-lane-count configurations now present subsystem ID 0144, and the lane count is reported separately.** 144-lane configurations are unaffected.

COMING FROM RC9 — RE-BASELINE AND FLASH BOTH IMAGES

PHY tuning, link-management microcode and core voltage all changed between RC9 and RC21, so link margins, equalization results, BER figures and power or thermal readings recorded on RC9 are not directly comparable with RC21 results.

Flash **both the miniSBR and the mainSBR** when upgrading from RC9. Coming from RC15 or RC18, only the mainSBR needs updating.